Using MDE for an Airborne FPGA Application

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Who are we?

- Eddie Power - Hardware Engineering Manager
- Tom Pitchforth - Hardware Engineer
- Alison Lucie - Senior Systems Engineer

- from SELEX Sensors & Airborne Systems in Edinburgh, UK.

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High Technology Defence Electronic Systems

Airborne Radar

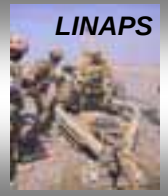

Seaspray 7000E

Electronic Warfare

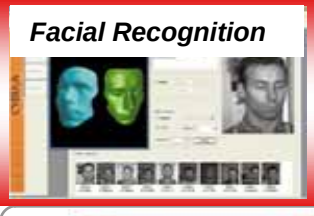
Electro-Optics


TIALD

Land Systems



MSI / APS / HLS



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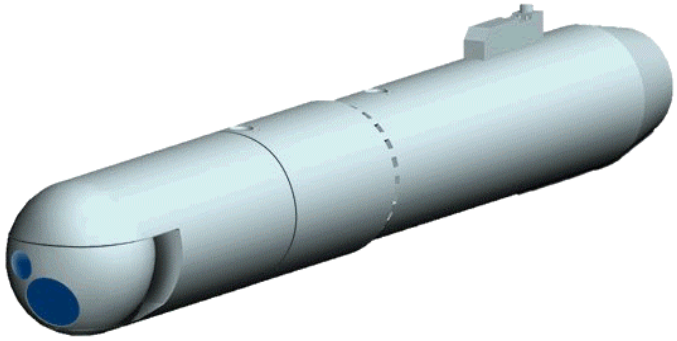
Why are we here ?

- **Majority of products contain custom in-house designed hardware.**
- **Into FPGAs in a big way - approx 50+ designs live at any time -**
  - SRAM, Flash and Anti-fuse
  - From 10K gate rad hard for satellites to multi-million gate Virtex.
- **Model Driven Engineering for targeting to FPGA now becoming mainstream for processing intensive applications.**
- **Preferred MDE toolset - Matlab/Simulink to FPGA via XILINX System Generator.**

JOANNA Advanced Targeting Pod

•FMMs for Targeting Pod
–Started as MEng Project to replace Analogue Controllers.
–Nallatech based prototype proved Controller Concept and MDE Implementation.
–Pod will fly with two custom controllers (WFoV and Steering Mirror).
–Papers on Mathworks web & in US COTS Journal.
–Presented at MDE UK 2005



Conclusions from JOANNA activities

"Bloody fantastic: analogue speed without analogue uncertainty, software capability without software overhead, rapid prototype without proprietary hardware." - Steve Gifford, Chief Systems Engineer

Tools are reasonably stable and usable in real applications

- Extension to existing design flow, not replacement.
- Complete end-to-end tool chain.
- Bolt-in to existing FPGA tools (Modelsim, Precision, P&R).
- Means of integrating design disciplines into common design env.

Big savings to be made by removing intermediate specification production and interpretation stage, reducing integration time and speeding-up design iterations.

Further applications

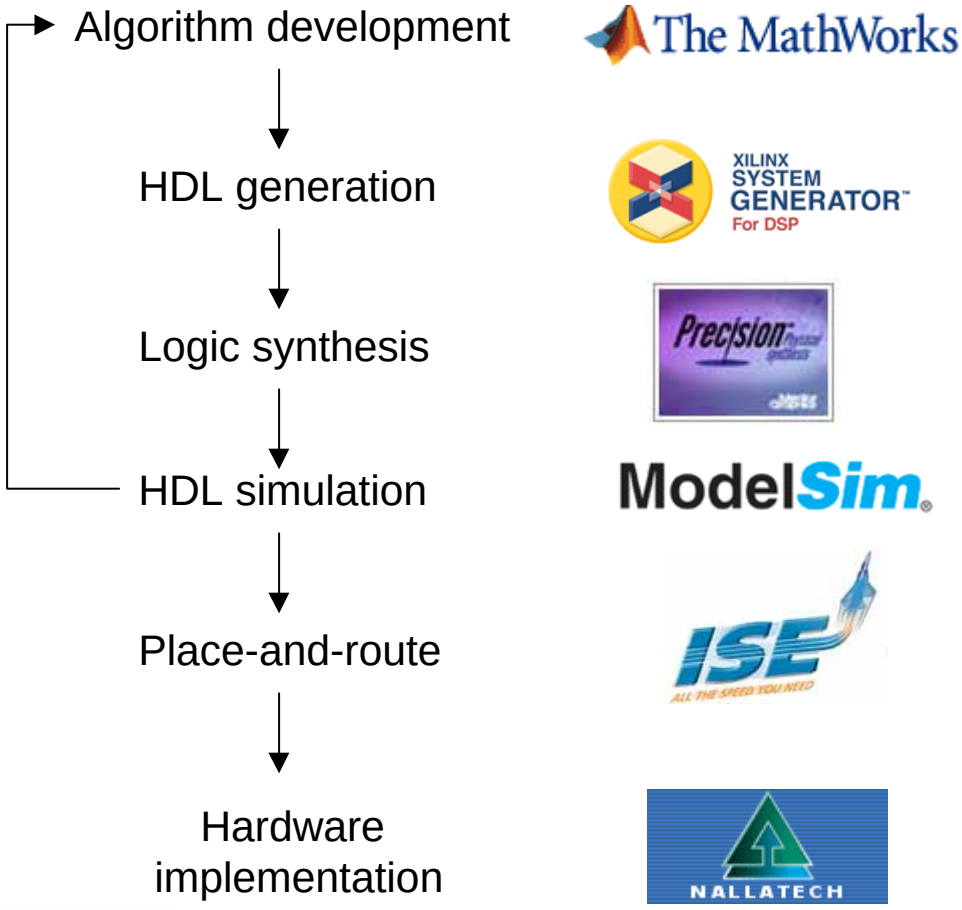
•RF Datalink

•RF Receiver Digitizer

•Image Processing -
Autofocus
Target Detection
Image Stabilization/Enhancement (7+ algs)

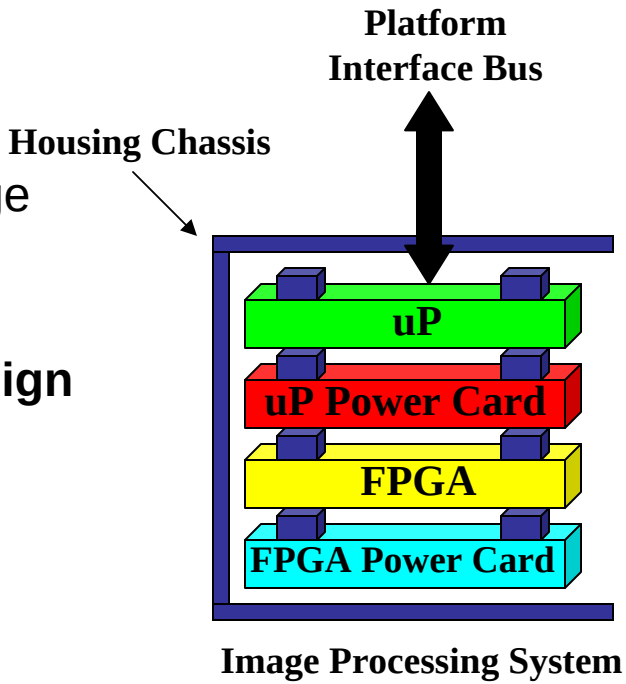
- Tools & process well embedded across patch.

System Generator Design Flow



Project Objectives

- **Current uP based design**
  - PC-104+ uP board and power card
  - Linux Operating System
  - 1 second to process sub-sampled 11Mpixel image
  - Intensity and size based filter

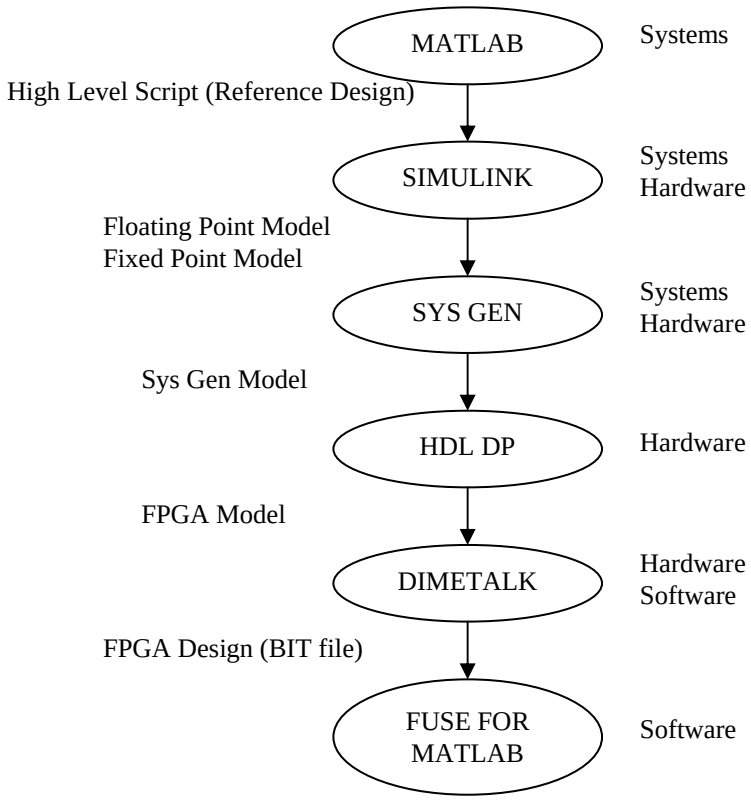


- **Convert Current uP design to an FPGA based design**
  - Relieve uP of main processing task
  - Reduce operating temperature of uP
  - Do not increase power consumption
  - Less than 1 second to process 11Mpixel image
  - Provide algorithm with equivalent/better processing results

- **Proposed FPGA based design**
  - Nallatech PC-104+ FPGA board and power card

Design Process

- **Matlab**
  - High Level Script
- **Simulink**
  - Floating Point Model
  - Fixed Point Model
- **Xilinx System Generator**
  - System Generator Model
- **HDL Designer Pro**
  - VHDL based Wrapper for FPGA design
- **Nallatech DIMETalk**
  - PCI interface and FPGA design
- **Nallatech FUSE for Matlab**
  - API functions to DMA data to/from FPGA card



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Design Procedure

- **High level Matlab scripting**
  - Rapid implementation to create reference design
  - Matlab scripts used in test-bench to perform additional tests
- **High level Floating-Point Simulink models**
  - Gradually broken down to simpler models
  - Enables easier translation to FPGA model
- **Lower level Fixed-Point Simulink models**
  - Quickly shows any differences between fixed-point and floating-point Models
- **Xilinx System Generator Model**
  - Can easily be tested alongside Fixed-Point Model to show differences
- **Hardware In the Loop (HIL) models used to target FPGA card**
  - Will indicate if there any discrepancies between theoretical FPGA model and actual hardware
- **HDL Designer Pro Wrapper**
  - Combines all Sys Gen ‘black boxes’ and can be simulated using Modelsim
- **DIMETalk Network**
  - Provides PCI interface and potential multi-FPGA networks
  - Easily accessed from Nallatech API functions
- **FUSE for Matlab**
  - Matlab equivalent of Nallatech C/C++ API functions
  - Allows main software to be created & tested in Matlab using the hardware

2D-FFT DEMO

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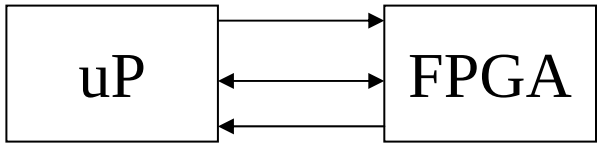
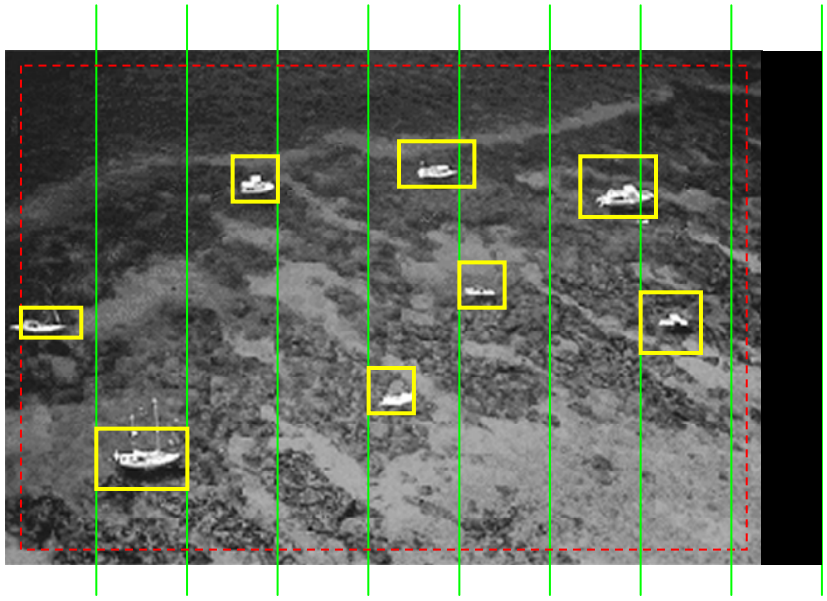
Design Overview





1. Section image so any image size is supported
   - Calculate useable region
   - Calculate each section
   - Ensure final section is correct size
2. DMA section to FPGA from uP
3. Read back results for the current section
4. Repeat steps 2 & 3 for every section
5. Create detection table using results
6. Return detection table to main program

DEMO

Actual Results

```
ATD_Registration...
Using ATD Algorithm ATD_FPGA
ATD Registration complete

Opening FPGA Card...
Configuring the FPGA...
Closing FPGA Card

ATD Initialisation...
Configuring the FPGA...
ATD Initialisation complete

# Processing Image ID 50

Total image transfer time = 0.451000 s

Total image sectioning time = 0.020000 s

atd_algorithm execution time = 0.451000 s

# ATD Found 8 detections in image ID 0
Obj ID  Img ID  tlx     tly     brx     bry     area    ndet    MatchVal
1       0       6       1434    234     1472    8931    88      1.406250
2       0       572     2007    885     2150    45216   45      1.527344
3       0       1228    632     1404    717     15222   50      1.480469
4       0       1998    1807    2144    1869    9261    30      1.179688
5       0       2193    578     2379    643     12342   29      1.117188
6       0       2492    1251    2604    1275    2825    34      1.320313
7       0       3207    689     3370    791     16892   36      1.281250
8       0       3503    1409    3658    1442    5304    55      1.410156

press <return> to exit.
```

****Small difference due to Floating-Point Vs Fixed-Point**

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Project Timescales

- **6 months for implementation & delivery (1 HW & 1 Systems Engineer)**
  - Card selection & initial hardware concepts – 1 month
  - Algorithm development & test (Matlab/Simulink) – 3 months
  - FPGA targeting & testing (HDL DP, DIMETalk, FUSE) – 2 months
  - Optimisations & delivery – 1 month
  - **Only 2 days required to translate FUSE code to ANSI C code
  - Less than 1 day to integrate into full system

Performance

	Detection > 90% (% test imagery)	FAR > 1 (% test imagery)
Customer	**73**	**74**
Selex-SAS	**91**	**5**

Algorithm Performance

- **Power consumption only slightly higher than previous system**
  - uP relieved of main processing task, so no longer running ‘white hot’
  - uP consuming less power
  - Only 48% of FPGA utilised

- **Processing Results**
  - Processing time of 350mS (LINUX) and 350mS (Windows)
    - 95% of which is DMA transfer time
  - uP equivalent processing time of 9000mS – FPGA was approx 30 times faster !!

Project Summary

- Project initially accepted on ‘best endeavours’ terms due to extreme timescales
  - Final product exceeded all expectations mainly due to the adopted design process
- Process resulted in Systems, Hardware & Software Engineers working closely
  - Quick turn around of requested design modifications
  - Programmable sensitivity parameters implemented in less than 1 day
  - Classification software designed in Matlab & compiled into dll format within 2 weeks
- Team of engineers more aware of constraints on other disciplines during design process
  - Same process has now been adopted for a much larger project on very tight timescales

Benefits of MDE flow

- Executable specification removes errors introduced by interpretation of requirements, cuts development time.
- Removal of “over-the-wall” approach resulting in better, faster communication between disciplines.
- Fast design iterations (e.g. effects of varying precision etc.).
- Direct correlation between simulation results and “real-world” performance
- Powerful device verification capability.
- Comprehensive system modeling environment.
- Raising the abstraction level reduces obsolescence issues.
- Expands skill set of all involved

Summary & Health Warning

- Wouldn't have taken on Image Processing projects without access to the tools.
- Lots of effort has been put in to get to "push button" stage.
- Lots of support from vendors (e.g. XILINX for autofocus).
- Worth the effort - now reaping rewards.
- "Autocoding" - sell tool on this basis to mgmt (verification is real benefit).
- All trad FPGA issues still there - Sync, timing, EMC, power cons, cooling.
- Still need HW & Systems & SW guys (work in same env with sensible overlap).
- Integrated tool-set expands horizons of all team members.